Total No. of Questions : 8]

SEAT No. :

PD-4096

[Total No. of Pages : 2

[6402]-56
S.E. (IT)
LOGIC DESIGN & COMPUTER ORGANIZATION
(2019 Pattern) (Semester - III) (214442)

Time : 2½ Hours] *[Max. Marks : 70*

Instructions to the candidates:

1) ***Answer Q1 or Q2, Q3 or Q4, Q5 or Q6, Q7 or Q8.***
2) ***Figures to the right indicate full marks.***
3) ***Assume Suitable data, if necessary.***

Q1) a) Draw and Explain in detail Internal diagram of Decade counter IC 7490. **[6]**

b) Differentiate between Synchronous Counter and Asynchronous Counter. **[6]**

c) Draw & Explain 3-bit Asynchronous Up-Counter using MS J-K flip flop (IC7476). **[5]**

OR

Q2) a) Draw Circuit diagram of 3-bit SIPO shift Register using D flip flop. Explain its working. **[6]**

b) List the various applications of Counter. **[6]**

c) Draw Pin Configuration of IC 7476.Explain the function of Preset and Clear. **[5]**

Q3) a) Design and explain Hardwired Control Unit. **[6]**

b) Explain in brief different functional units of computer system. **[6]**

c) What are the typical registers in a CPU? State the purpose of each type of registers. **[6]**

OR

P.T.O.

Q4) a) Explain and draw basic structure of Harvard architecture. Write the difference between Harvard and Von Neumann architecture. **[6]**

b) Write micro-operations for any **ONE** : fetch, indirect, execute, interrupt **[6]**

c) Draw & explain typical organization of microprogrammed control unit. **[6]**

Q5) a) What is mean by Instruction format? Explain 0-1-2-3 address formats with suitable example? **[6]**

b) What is meant by Machine Instruction? Explain various Operand types used in Machine Instruction. **[6]**

c) Draw and explain Symmetric Multiprocessors Architectures. **[5]**

OR

Q6) a) Differentiate between RISC and CISC Architecture. **[6]**

b) What is mean by interrupt? Explain step by step interrupt handling procedure of microprocessors. **[6]**

c) List the advantages & applications of multiprocessor systems. **[5]**

Q7) a) Draw Memory Hierarchy. What is the objective of organizing different memories at the different hierarchy? **[6]**

b) Consider a cache consisting of 16 words. Each block consists of 4 words. Size of main memory is 256 bytes. Find number of bits in each of the TAG & WORD fields for fully associative mapped cache. **[6]**

c) Write a note on any **ONE** : Programmed I/O, Interrupt Driven I/O. **[6]**

OR

Q8) a) Along with suitable diagram explain set associative cache mapping technique. **[6]**

b) Along with suitable diagram explain following cache Write Strategies:
i) Write Through ii) Write Back **[6]**

c) Describe the typical signals used to connect memory to processor. **[6]**