Total No. of Questions—**8**] [Total No. of Printed Pages—**2**

Seat No.	

[5559]-203

S.E. (IT) (First Semester) EXAMINATION, 2019

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. :- 1) Answer questions 1 **or** 2, 3 **or** 4, 5 **or** 6, and 7 **or** 8.
2) Neat diagrams must be drawn wherever necessary.
3) Assume suitable data, if necessary

1. (a) Convert given numbers in binary form and use 2's complement method to perform following operations [6]
i) (- 48) – (+23) ii) - (48) – (- 23)

(b) Design and implement 8:1MUX using two 4:1 mux and implement given function. [6]
F(X, Y, Z) = Σ m (1,3,4,7)

OR

2 (a) Explain with diagram CMOS to TTL interface [6]

(b) Use K-map minimization technique to realize following expression using minimum number of gates. [6]
Y = = Σ m (1, 2, 9, 10, 11, 14, 15)

3 (a) Design MOD 93 counter using IC 7490. [6]

(b) Draw and explain SISO and PIPO type of shift register. Give application of each. [6]

OR

4 (a) Draw JK Flip flop using gates and explain Race around condition with the help of timing diagram. [6]

(b) A sequential digital system has input pin P and output Q. Output Q becomes 1 only when three consecutive '1's are received on pin P. Design the circuit using D flip flops and Moore modeling style. [6]

P.T.O.

5 (a) Draw and explain general structure of PLA. [6]

(b) Draw the ASM chart for 2 bit binary counter having enable input E such that if E =1, counting enables and for E =0 counting disables and starts from initial state. [7]

OR

6 (a) Implement following function using suitable PAL. F(A,B,C,D) = Σ m(0,1,3,15) [7]

(b) Compare PROM, PLA and PLA devices. [6]

7 (a) Write VHDL code (Entity and Architecture) for 4:1Multiplexer using Dataflow modeling style. [6]

(b) Explain structure of VHDL code and explain its various components. [7]

OR

8 (a) Compare Behavioural, Dataflow and Structural modeling styles in VHDL programming. [6]

(b) Write VHDL code for Half adder using Behavioural modeling style. [7]