Total No. of Questions : 4]

SEAT No. :

PD291

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B.E. (E & TC Engineering) (Insem)

NANO ELECTRONICS

(2019 Pattern) (Semester-VIII) (Elective-VI) (404192 B)

Time : 1 Hour] *[Max. Marks : 30*

Instructions to the candidates:

1) ***Answer Q.1 or Q.2, Q.3 or Q.4.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data if necessary.***

Q1) a) Name the tools for measuring Nano structure? Explain Transmission Electron Microscope(TEM). **[8]**

b) Explain Scanning Prob Microscopy (SPM) With neat Diagram. **[7]**

OR

Q2) a) What are the limitation of Silicon Materials. **[7]**

b) Explain Lithography Process Steps. **[8]**

Q3) a) Explain Dielectric Material for future Transistor. **[8]**

b) Explain Atomic Force Microscopy (AFM). **[7]**

OR

Q4) a) With Neat diagram Explain Nano CMOS-Devices. **[7]**

b) Explain Silicon nano Crystal Non Volatile Memories. **[8]**