| Total | l No. | of Questions : 8] SEAT No. : |] | | |
|--------------------------|-------|---|---|--|--|
| P47 | 766 | [Total No. of Pages : 2 | ! | | |
| | | [5561]-650 | | | |
| | | B.E. (E & TC) | | | |
| VLSI Design & Technology | | | | | |
| (2015 Pattern) | | | | | |
| | | | | | |
| Tim | e:2 | ½ Hours] [Max. Marks: 70 |) | | |
| Instr | | ons to the candidates : | | | |
| | 1) | All questions are compulsory. | | | |
| | 2) | Figures to the right indicate full marks. | | | |
| 01) | ` | | | | |
| Q1) | a) | Explain procedure with the help of VHDL code. [6] | | | |
| | b) | Explain clock skew and methods to minimize the effect of clock skew. | | | |
| | | | | | |
| | c) | Explain any four important specifications of FPGA. Also explain CLB's in FPGA. | | | |
| | | | | | |
| | | OR | | | |
| <i>Q2</i>) | a) | Explain VHDL attributes with example. [6] | | | |
| | b) | Explain interconnect Routing Techniques. [7] | 0 | | |
| | c) | Explain in detail architecture of Macrocell in CPLD. [7] | V | | |
| | | | | | |
| Q3) | a) | Explain the following: [8] | | | |
| ~ / | ĺ | i) Body Effect | | | |
| | | ii) Hot Electron Effect | | | |
| | 1.) | | | | |
| | b) | Derive the expression for static & Dynamic power dissipations. Compare them. [8] | | | |
| | | OR OR | | | |
| 0 (1) | ` | | | | |
| Q4) | a) | Design CMOS logic for $\gamma = ABC + D$. Calculate W/L ratio for NMOS & PMOS area needed on chip. [8] | | | |
| | b) | Draw & explain CMOS transfer characteristics. [8] | | | |
| | U) | Diam & explain civios transfer characteristics. | | | |

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| Q5) a) | Explain cross talk and drain punch through. | [8] |
|---------------|--|------------|
| b) | Explain fabrication method of CMOS using n well process. | [10] |
| | OR | |
| Q6) a) | Explain Design issues like antenna effect and electro migration | effcct.[8] |
| b) | Draw stick diagram for CMOS inverter, NAND, NOR gate. | [10] |
| | | 6 |
| Q7) a) | Explain TAP controller with state diagram. | [8] |
| b) | Write short note on BIST. | [8] |
| | OR | |
| Q8) a) | Explain JTAG in detail. | [8] |
| b) | Explain in detail stuck at fault model. | [8] |
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