Total No. of Questions—**8**] [Total No. of Printed Pages—**2**

Seat No.	

[5559]-137

S.E. (E & TC/Electronics) (I Sem.) EXAMINATION, 2019
DIGITAL ELECTRONICS
(2015 PATTERN)

Time : Two Hours **Maximum Marks : 50**

Instructions to the candidates:

1) *Attempt Q.1 or Q.2, Q.3 or Q.4, Q.5 or Q.6, Q.7 or Q.8.*
2) *Neat diagrams must be drawn wherever necessary.*
3) *Figures to the right indicate full marks.*
4) *Assume suitable data, if necessary.*
5) *Use of logarithmic tables, slide rule and electronic non programmable calculator is allowed.*

Q1	a.	Design 3 bit binary to grey code converter	06
	b	Convert D F/F to J/K F/F	06
		OR	
Q2	a	Design Even bit parity checker	06
	b	Design 3 bit twisted ring counter	06
Q3	a	Design sequence detector to detect..10110..	06
	b	Give comparisons between TTL, ECL and CMOS logic families	04
	c	Draw and explain SR Flip Flop using NAND gates.	02
		OR	
Q4	a	Draw and explain TTL to CMOS interface.	06
	b	Compare Moor and Mealy Machine	04
	c	What is Clock Skew and Clock jitter?	02
Q5	a	Implement following using PLA F1 = AB'+AC+A'BC' F2 = (AC+BC)	06
	b	List Various semiconductor memory with their characteristic.	07

P.T.O.

OR

Q6	a	Explain PROM with diagram	06
	b	List Various Programmable logic Devices with their characteristic	07
Q7	a	List & explain Mode of Timer/ Counter for 8051	05
	b	Write short note on 8051 feature	04
	c	Mention any four addressing modes of 8051?	04

OR

Q8	a	Draw and explain Program Status Word	05
	b	Compare Microcontroller & Microprocessor	04
	c	Explain the Instruction for arithmetic's with examples	04