

Total No. of Questions : 4]

SEAT No. :

PA-11

[Total No. of Pages : 2

[5931]-17

S.E. (Electrical)

ANALOG & DIGITAL ELECTRONICS
(2019 Pattern) (Semester - I) (203143)

Time : 1 Hour

[Max. Marks : 30

Instructions to the candidates:

- 1) Solve Q1 or Q2, Q3 or Q4.
- 2) Figures to the right indicate full marks.
- 3) Neat diagrams must be drawn wherever necessary.
- 4) Assume suitable data, if necessary.

Q1) a) Plot the following Boolean expressions on K Map [5]

$$\begin{aligned} \text{i)} \quad Y &= ABC + \overline{A}\overline{B}C + A\overline{B}\overline{C} \\ \text{ii)} \quad Y &= \overline{A}\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}\overline{D} + \overline{ABC}\overline{D} + A\overline{B}CD + ABC\overline{D} \end{aligned}$$

b) Minimize the following Boolean function-using K Map [5]

$$F(A, B, C, D) = \sum m(0, 1, 3, 5, 7, 8, 9, 11, 13, 15)$$

c) Describe the function of half adder with its logic diagram and truth table. [5]

OR

Q2) a) Draw logical diagram of 8:3 encoder. Explain its working with truth table. [5]

b) Prove the following using the Boolean algebra theorems [5]

$$\text{i)} \quad A + \overline{A} \cdot B + A \cdot \overline{B} = A + B$$

$$\text{ii)} \quad A \cdot B + \overline{A} \cdot B + \overline{A} \cdot \overline{B} = \overline{A} + B$$

c) What is meant by SOP and POS form of reduction? Explain one with example. [5]

P.T.O.

- Q3)** a) State difference between synchronous and asynchronous counters (5 points). [5]
- b) Draw and explain Asynchronous Up-Down counter. [5]
- c) What is meant by shift register? List different types of shift register. [5]

OR

- Q4)** a) Design and explain the operation of MOD 10 asynchronous counter. [5]
- b) Explain twisted ring counter in detail with truth table. [5]
- c) Draw circuit diagram and explain 4 bit universal shift register. [5]

