Total No. of Questions : 4]

SEAT No. :

**PC403**

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**[6359]-523**

# S.E. (Computer Engineering) (Insem)

## DIGITAL ELECTRONICS AND LOGIC DESIGN

## (2019 Pattern) (Semester- III) (210245)

*Time : 1 Hour]* *[Max. Marks : 30*

***Instructions to the candidates:***

1) ***Attempt Q1 or Q2, Q3 or Q4.***
2) ***Neat diagram must be drawn wherever necessary.***
3) ***Assume suitable data, if necessary.***

***Q1)*** a) Solve the following equation using K-map minimization techniques. Also draw the diagram using basic gates

$F(A,B,C,D)=\Sigma m\ (2,7,8,10,11,13,15)$ **[5]**

b) Minimize the function in POS form and also draw the diagram

$F(A,B,C,D)=\pi M(0,1,3,5,6,7,9,10,15)$ **[5]**

c) How will you implement full adder using half adder? Explain the circuit diagram. **[5]**

OR

***Q2)*** a) Represent the following decimal numbers in **[5]**

i) Sign magnitude form

ii) Sign 1's complement form

iii) Sign 2's complement form

1) +14
2) +27
3) –17
4) +45

b) Minimize the following logic function using K-map and realize using logic gates. Draw the diagram $F(A,B,C,D)= \Sigma m(1,3,7,11,15)+d(0,2,5)$ **[5]**

c) Simplify logic equation using Quine Mc Cluskey minimization Technique $Y(A,B,C,D)= \Sigma m(0,1,3,7,8,9,11,15)$ **[5]**

***P.T.O.***

***Q3)*** a) Design and Implement 4 bit Binary to Gray code converter using logic gate. **[5]**

b) Design single digit BCD adder using 4 Bit binary adder IC 7483. **[5]**

c) Implement the expression using a 8:1 multiplexer

$F(A,B,C,D)=\Sigma m(0,2,3,6,8,9,12,14)$ **[5]**

OR

***Q4)*** a) Write a short note on look ahead carry generator also explain its importance. **[5]**

b) Design 2-bit magnitude comparator using logic gates. **[5]**

c) Design 3 bit parity generator circuit using odd parity bit. **[5]**